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S18	0	("wo2001424").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/16 13:04

S19	6	(("5600579") or ("5838948") or ("6052524")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/16 13:05
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1. **Reuse issues in SoC verification platform**
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Terms used **soc verification BIST**

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1 Test (co-organized with LA-TTTC): Improving mixed-signal SOC testing: a power-aware reuse-based approach with analog BIST

Antonio Andrade, Erika Cota, Marcelo Lubaszewski

September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**

Full text available: pdf(163.20 KB) Additional Information: full citation, abstract, references, index terms

Analog BIST and SoC testing are two topics that have been extensively, but independently, studied in the last few years. However, current mixed-signals systems require the combination of these subjects to generate a cost-effective test solution for the whole SoC. This paper discusses the impact on the global system testing time of an analog BIST method based on digital reuse. Experimental results show that the reuse of digital blocks to test analog signals is indeed a very efficient strategy, ev ...

Keywords: BIST, mixed-signal test, power aware, system-on-chip

2 HiBRID-SoC: A Multi-Core System-on-Chip Architecture for Multimedia Signal Processing Applications

Hans-Joachim Stolberg, Mladen Berekovic, Lars Friebe, Soren Moch, Sebastian Flugel, Xun Mao, Mark B. Kulaczewski, Heiko Klusmann, Peter Pirsch

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe: Designers' Forum - Volume 2 DATE '03**

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The HiBRID-SoC multi-core system-on-chip targets a wide range of application fields with particularly high processing demands, including general signal processing applications, video and audio de-/encoding, and a combination of these tasks. For this purpose, the HiBRID-SoC integrates three fully programmable processors cores and various interfaces onto a single chip, all tied to a 64-Bit AMBA AHB bus. The processor cores are individually optimized to the particular computational characteristics ...

3 A computer aided engineering system for memory BIST

Chauchin Su, Shih-Ching Hsiao, Hau-Zen Zhau, Chung-Len Lee

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**